INTERSIL
SYSTEMS DIVISION

ISB-3600 Arithmetic Card

772

FEATURES

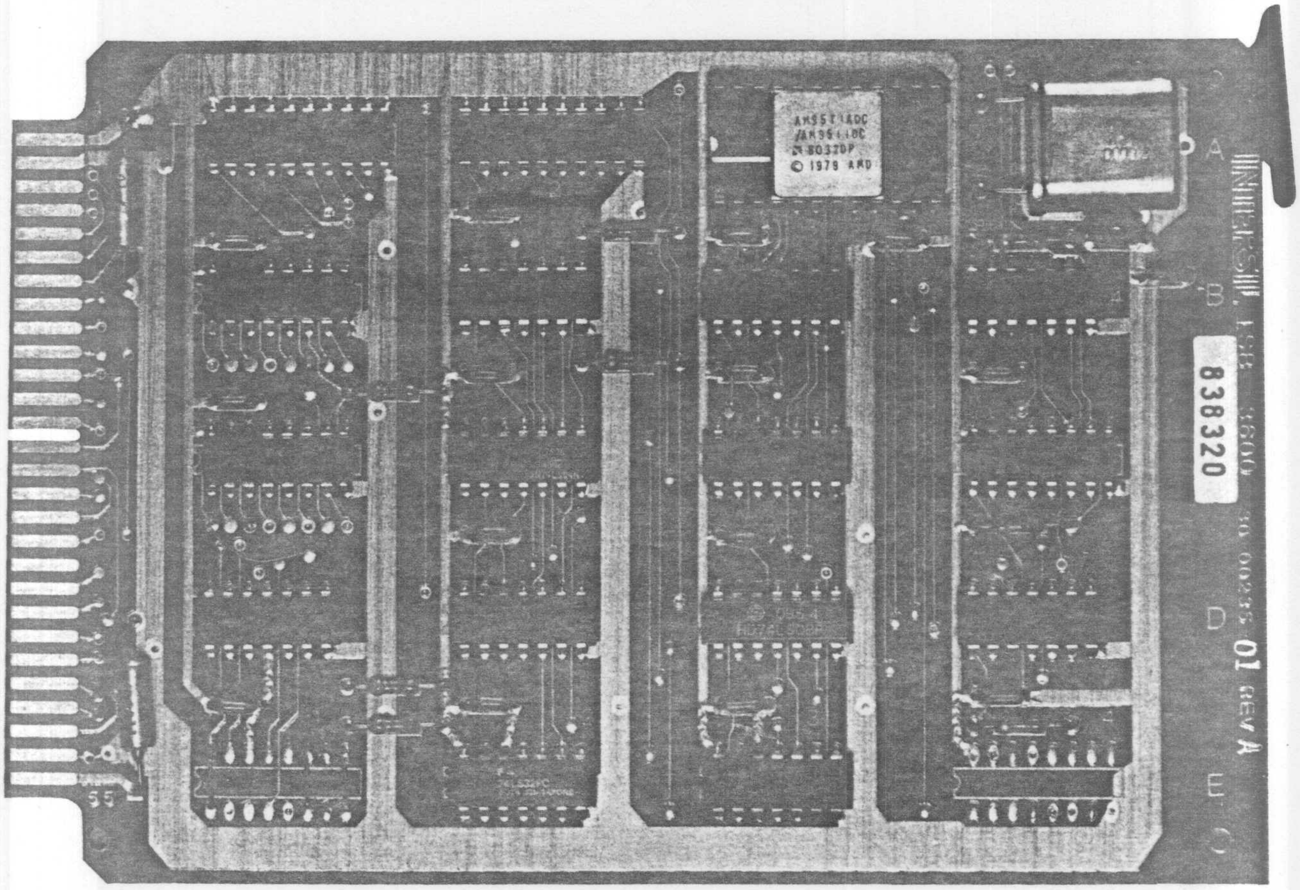
- Full STD BUS Compatibility
- Binary Data Format
- Fixed Point 16 and 32 Bit Operations
- Floating Point 32 Bit Operations
- Add, Subtract, Multiply and Divide
- Trigonometric and Inverse Trigonometric Functions
- Square Root, Logarithms, Exponentials
- Floating to Fixed and Fixed to Floating Conversions
- Stack Oriented Operand Storage
- Software Programmable Vectored or Polling Type Interrupts
- Customer Selectable Port Address
- Voltage Requirements: +5V, +12V

GENERAL DESCRIPTION

The ISB-3600 is a STD BUS Arithmetic Processor card that provides a STD BUS Microprocessor System with high-speed arithmetic and trigonometric computation capability. The card will operate with either the Z80 based ISB-3100 or the 8085 based ISB-3110 Central Processor Cards.

Using a monolithic MOS/LSI device, the card provides high performance fixed and floating point arithmetic operations and a variety of floating point trigonometric and mathematical operations. Operands are pushed onto an internal stack and a command is issued to perform operations on the data in the stack. Results are then available to be retrieved from the stack or additional commands may be entered.

The Arithmetic card uses 4 consecutive I/O address locations. The 4 address locations are decoded from the lower 2 address bits. The top 6 address bits are customer assignable.



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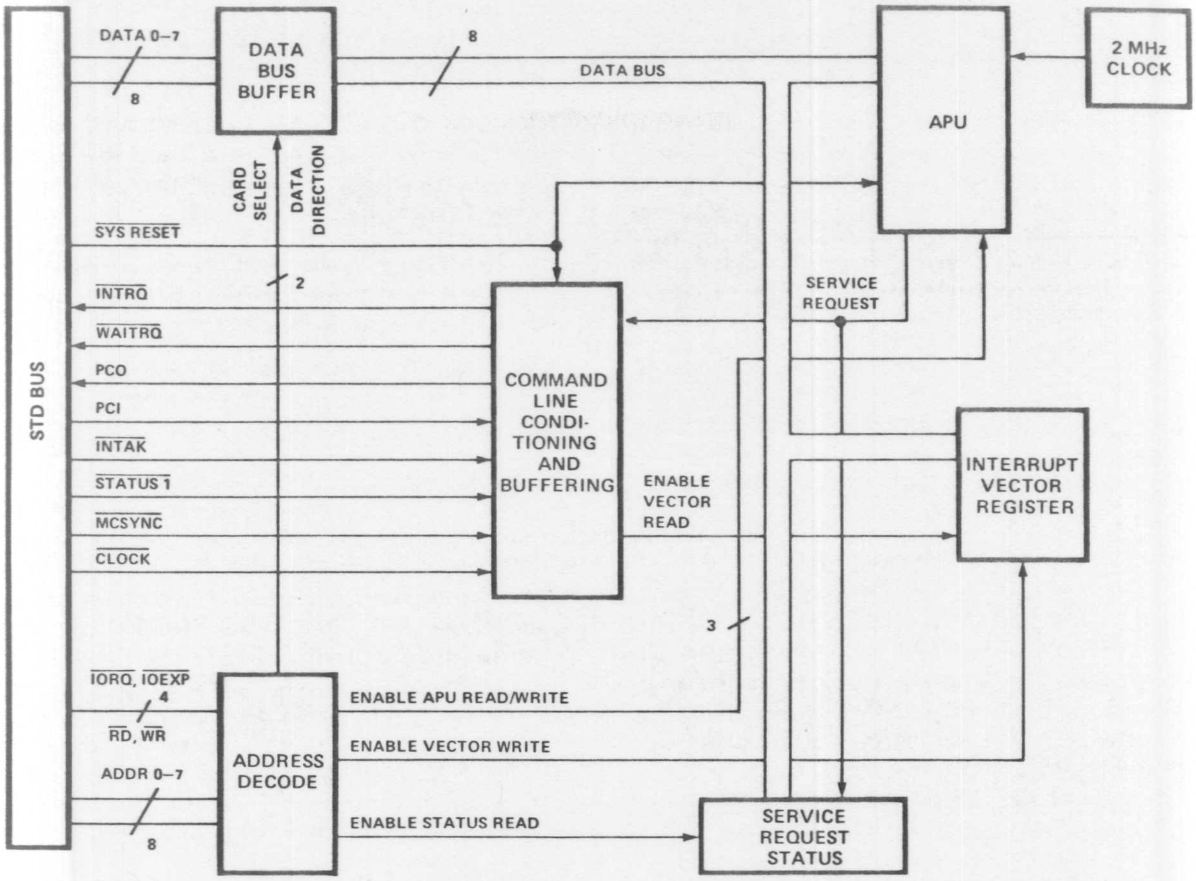


FIGURE 1. ISB-3600 Block Diagram

SPECIFICATIONS

Word Size:	8 Bits
Arithmetic Functions:	Arithmetic/Trigonometric/Exponential Functions with both fixed all floating point operations
I/O Address Selection:	Lowest Port Address Selectable within the Range of 00 and FC, in Increments of 4
Interface:	All Address, Data, and Command Signals are TTL Compatible
Power Requirements:	+5 VDC at 0.42 Amp max. +12 VDC at 0.09 Amp max.
Mating Connectors:	See Table 1
Card Dimensions:	Height 6.5 inches (16.51 cm) Width 4.48 inches (11.38 cm) Thickness: 0.442 inches (1.122 cm)

ENVIRONMENTAL REQUIREMENTS

Operating Temperature:	0° to 55°C
Storage Temperature:	–40° to 80°C
Relative Humidity:	0% to 90% without condensation

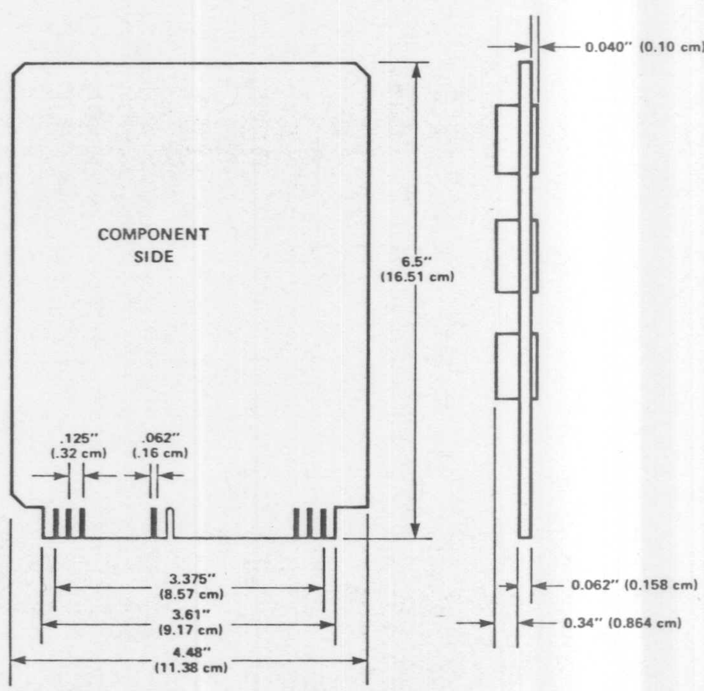


FIGURE 2. ISB-3600 Physical Card Dimensions

TABLE 1. ISB-3600 Compatible Mating Connectors

INTERFACE	NO. OF PINS	CENTERS	CONNECTOR TYPE	VENDOR	VENDOR PART NO.	KEYED
STD BUS	56	0.125 in.	Solder Tail	Viking Winchester	VH28/ICNK5 2HW D0–111	Between Pins 26 and 28
STD BUS	56	0.125 in.	Wire Wrap	Viking Winchester	VH28/ICND5 HW28 D0–111	

TABLE 2. ISB-3600 STD BUS Organization and Functional Specifications (With Pin Definitions)

The STD BUS pinout is organized into five functional groups:

Logic Power Bus	Pins 1–6
Data Bus	Pins 7–14
Address Bus	Pins 15–30
Control Bus	Pins 31–52
Auxiliary Power Bus	Pins 53–56

COMPONENT SIDE				CIRCUIT SIDE			
PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION
1	+5V	In	+5 Volts DC (Bussed)	2	+5V	In	+5 Volts DC (Bussed)
3	GND	In	Digital Ground (Bussed)	4	GND	In	Digital Ground (Bussed)
5	–5V	In	–5 Volts DC	6	–5V	In	–5 Volts DC
7	D3	In/Out	Low Order Data Bus	8	D7	In/Out	High Order Data Bus
9	D2	In/Out	Low Order Data Bus	10	D6	In/Out	High Order Data Bus
11	D1	In/Out	Low Order Data Bus	12	D5	In/Out	High Order Data Bus
13	D0	In/Out	Low Order Data Bus	14	D4	In/Out	High Order Data Bus
15	A7	Out	Low Order Address Bus	16	A15	Out	High Order Address Bus
17	A6	Out	Low Order Address Bus	18	A14	Out	High Order Address Bus
19	A5	Out	Low Order Address Bus	20	A13	Out	High Order Address Bus
21	A4	Out	Low Order Address Bus	22	A12	Out	High Order Address Bus
23	A3	Out	Low Order Address Bus	24	A11	Out	High Order Address Bus
25	A2	Out	Low Order Address Bus	26	A10	Out	High Order Address Bus
27	A1	Out	Low Order Address Bus	28	A9	Out	High Order Address Bus
29	A0	Out	Low Order Address Bus	30	A8	Out	High Order Address Bus
31	$\overline{\text{WR}}$	Out	Write to Memory or I/O	32	$\overline{\text{RD}}$	Out	Read to Memory or I/O
33	$\overline{\text{IORQ}}$	Out	I/O Address Select	34	$\overline{\text{MEMRQ}}$	Out	Memory Address Select
35	$\overline{\text{IOEXP}}$	In/Out	I/O Expansion	36	$\overline{\text{MEMEX}}$	In/Out	Memory Expansion
37	$\overline{\text{REFRESH}}$	Out	Refresh Timing	38	$\overline{\text{MCSYNC}}$	Out	CPU Machine Cycle Sync
39	$\overline{\text{STATUS 1}}$	Out	CPU Status	40	$\overline{\text{STATUS 0}}$	Out	CPU Status
41	$\overline{\text{BUSAK}}$	Out	Bus Acknowledge	42	$\overline{\text{BUSRQ}}$	In	Bus Request
43	$\overline{\text{INTAK}}$	Out	Interrupt Acknowledge	44	$\overline{\text{INTRQ}}$	In	Interrupt Request
45	$\overline{\text{WAITRQ}}$	In	Wait Request	46	$\overline{\text{NMIRQ}}$	In	Non-Maskable Interrupt
47	$\overline{\text{SYSRESET}}$	Out	System Reset	48	$\overline{\text{PBRESET}}$	In	Push Button Reset
49	$\overline{\text{CLOCK}}$	Out	Clock from Processor	50	$\overline{\text{CNTRL}}$	In	AUX Timing
51	PCO	Out	Priority Chain Out	52	PCI	In	Priority Chain In
53	AUX GND	In	AUX Ground (Bussed)	54	AUX GND	In	AUX Ground (Bussed)
55	AUX+V	In	AUX Positive (+12 Volts DC)	56	AUX–V	In	AUX Negative (–12 Volts DC)

TABLE 3. ISB-3600 STD BUS Signal Definitions

SIGNAL	PIN NO.	FUNCTIONAL DESCRIPTION
+5V	1 & 2	*+5 Logic Voltage (V_{CC})* – Main logic voltage lines (+5 volts). Both pins are bussed together for current capacity.
GND	3 & 4	*Logic Ground* – Ground for logic power. Both pins are bussed together for current capacity.
–5V	5 & 6	*–5 Logic Voltage* – Both pins are bussed together for current capacity. (Not used on the ISB-3600).
D0–D7	7–14	*Data Bus* – An 8-Bit bidirectional tri-state bus. (Bidirectional means signals may flow either into or out of any card on the Bus). Direction of data is normally controlled by the processor card via the Control Bus. The data direction is normally affected by such signals as Read ($\overline{RD}$), Write ($\overline{WR}$) and Interrupt Acknowledge ($\overline{INTAK}$). The Data Bus uses high-level active logic levels. All cards are required to release the bus to a high impedance state when not in use. The Processor card releases the data bus in response to Bus Request ($\overline{BUSRQ}$) input from an alternate system controller, as in DMA transfers.
A0–A15	15–30	*Address Bus* – A 16-bit tri-state high-level active bus. The address will originate at the processor card or a bus controlling device. The processor card releases the Address Bus in response to a Bus Request ($\overline{BUSRQ}$) input from an alternate controller. The Address Bus provides 16 address lines for decoding by either memory or I/O. Memory request ($\overline{MEMRQ}$) and I/O request ($\overline{IORQ}$) control lines are used to distinguish between the two operations. The ISB-3600 uses only the lower 8 bits during an I/O request operation.
$\overline{WR}$	31	*Write to Memory or I/O* – A tri-state, active-low control line that indicates the BUS holds valid data to be written in the addressed memory or output device. The ISB-3600 is an I/O device only.
$\overline{RD}$	32	*Read from Memory or I/O* – A tri-state, active-low control line that indicates the processor or other bus controlling device wants to read data from memory or an I/O device. The selected I/O device or memory should use this signal to gate data onto the BUS. The ISB-3600 is an I/O device only.
$\overline{IORQ}$	33	*I/O Address Select* – A tri-state, active-low processor output control line. $\overline{IORQ}$ indicates that the address lines hold a valid I/O address for an I/O Read or Write.
$\overline{MEMRQ}$	34	*Memory Address Select* – A tri-state, active-low memory request line. $\overline{MEMRQ}$ indicates that the Address Bus holds a valid address for memory read or memory write operations. (Not used on the ISB-3600).
$\overline{IOEXP}$	35	*I/O Expansion* – An active-low control signal used to expand or enable I/O Port addressing.
$\overline{MEMEX}$	36	*Memory Expansion* – An active-low control signal used to expand or enable memory addressing. (Not used on the ISB-3600).
$\overline{REFRESH}$	37	*Dynamic Memory Refresh* – a tri-state, active-low control line normally used to refresh dynamic memory. This signal is generated on the processor card. (Not used on the ISB–3600).
$\overline{MCSYNC}$	38	*Machine Cycle Sync* – A tri-state, active-low processor output signal that occurs once during each processor machine cycle. (Machine cycle is defined as the sequence that involves Addressing, Data Transfer and Execution.) $\overline{MCSYNC}$ defines the beginning of the machine cycle. The ISB-3600 uses this line to start priority identification and wait state generation in an 8085 processor system.
$\overline{STATUS\ 1}$	39	*Status Control Line 1* – The ISB-3600 uses this line to start priority identification in a Z80 processor system.

TABLE 3. ISB-3600 STD BUS Signal Definitions (Continued)

SIGNAL	PIN NO.	FUNCTIONAL DESCRIPTION
$\overline{\text{STATUS 0}}$	40	*Status Control Line 0* – Status Control lines provide timing information related to special cycle operations. (Not used on the ISB-3600).
$\overline{\text{BUSAK}}$	41	*BUS Acknowledge* – An active-low output line. The processor responds to a $\overline{\text{BUSRQ}}$ by releasing the BUS and giving an Acknowledge signal on the $\overline{\text{BUSAK}}$ line. $\overline{\text{BUSAK}}$ occurs at the completion of the current machine cycle. (Not used on the ISB-3600).
$\overline{\text{BUSRQ}}$	42	*Bus Request* – An active-low input line. A $\overline{\text{BUSRQ}}$ causes the processor to suspend operations on the BUS by releasing all tri-state BUS lines for use by another processor. The BUS is released once the current machine cycle is completed. (Not used on the ISB-3600).
$\overline{\text{INTAK}}$	43	*Interrupt Acknowledge* – An active-low output line from the processor card that occurs in response to ($\overline{\text{INTRQ}}$). It is used to tell the interrupting device that the processor card is ready to respond to the Interrupt. For vectored interrupts the vector address is placed on the Data Bus by the interrupting device during $\overline{\text{INTAK}}$. The ISB-3600 will output a vector address on the Data Bus if it is the highest priority card.
$\overline{\text{INTRQ}}$	44	*Interrupt Request* – An active-low processor card input line that conditionally interrupts the program. It is masked and ignored by the processor unless deliberately enabled by a program instruction. If the processor accepts the interrupt, it acknowledges by dropping $\overline{\text{INTAK}}$. If programmed, the ISB-3600 uses this line to interrupt the processor when it is done with an operation.
$\overline{\text{WAITRQ}}$	45	*Wait Request* – An active-low input line to the processor that suspends processor operations as long as it remains low. The processor will hold in a state that maintains a Valid Address on the Address Bus. The ISB–3600 generates wait requests during I/O requests.
$\overline{\text{NMIRQ}}$	46	*Non-Maskable Interrupt* – An active-low processor card interrupt input line of highest priority. (Not used on the ISB–3600).
$\overline{\text{SYSRESET}}$	47	*System Reset* – An active-low output from the system reset circuit. The system reset circuit is triggered by power-on detection or by the pushbutton reset. The system reset bus line should be applied to all cards on the BUS that have latch circuits requiring initialization. On the ISB-3600, the APU, Interrupt Logic, Wait Request Logic and Lock Out Logic is reset.
$\overline{\text{PBRESET}}$	48	*Push Button Reset* – An active-low input line to the system reset circuit. (Not used on the ISB–3600).
$\overline{\text{CLOCK}}$	49	*Clock From Processor* – A buffered processor clock signal used for system synchronization or as a general clock source. The ISB–3600 uses this line to control the wait state generation circuitry in an 8085 processor system.
$\overline{\text{CNTRL}}$	50	*Control* – An external clock input for special clock timing. (Not used on the ISB–3600).
PCO	51	*Priority Chain Output (Output, active-high)* – This signal is sent to the PCI input of the next lower card in the priority chain. A card that needs priority should hold PCO low.
PCI	52	*Priority Chain In (Input, active-high)* – This signal is provided directly from the PCO of the next higher card in the priority chain. A high level on PCI gives priority to the card sensing the PCI input.
AUX GND	53 & 54	*Auxiliary Ground* – Ground for AUX Power. Both pins bussed together for current capacity.
AUX +V	55	*Auxiliary Positive Voltage (+12 Volts DC)*
AUX –V	56	*Auxiliary Negative Voltage (–12 Volts DC)* – (Not used on the ISB–3600)

TABLE 4. ISB-3600 Arithmetic Command Summary

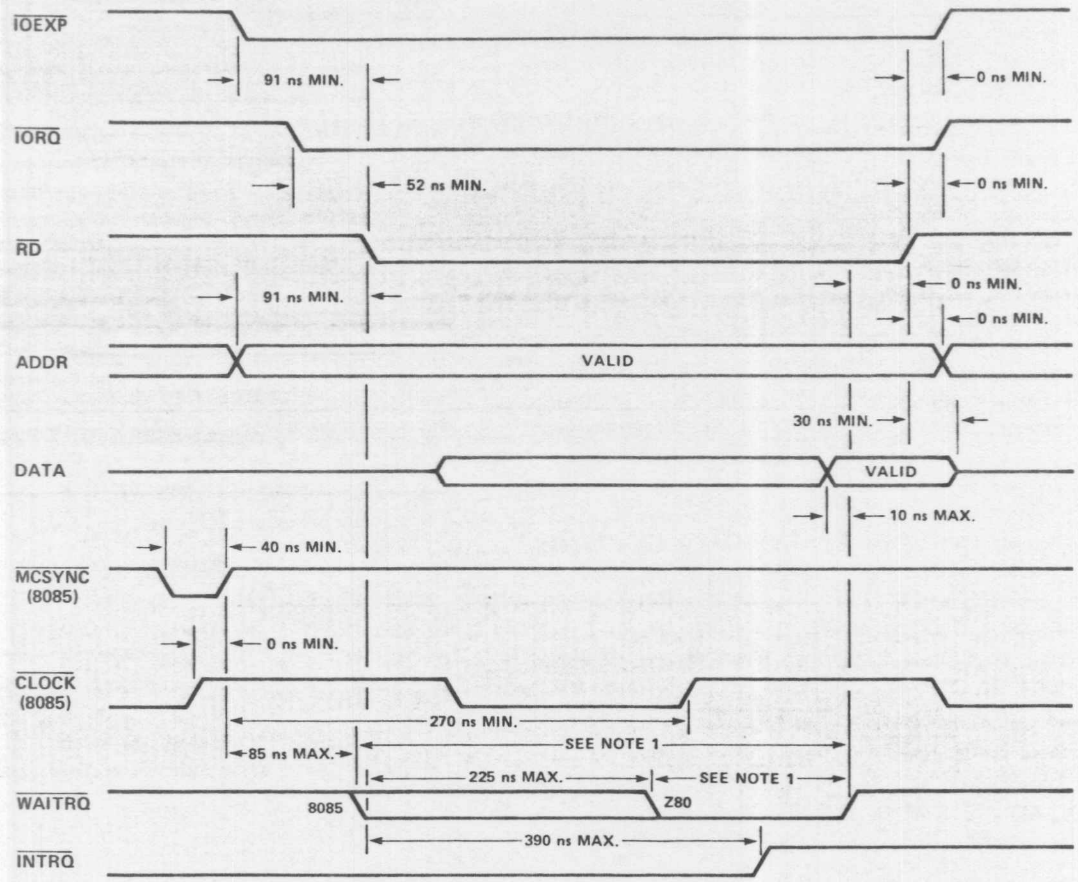
COMMAND MNEMONIC	COMMAND DESCRIPTION
FIXED POINT 16 BIT	
SADD	Add TOS to NOS. Result to NOS. Pop Stack.
SSUB	Subtract TOS from NOS. Result to NOS. Pop Stack.
SMUL	Multiply NOS by TOS. Lower half of result to NOS. Pop Stack.
SMUU	Multiply NOS by TOS. Upper half of result to NOS. Pop Stack.
SDIV	Divide NOS by TOS. Result to NOS. Pop Stack.
FIXED POINT 32 BIT	
DADD	Add TOS to NOS. Result to NOS. Pop Stack.
DSUB	Subtract TOS from NOS. Result to NOS. Pop Stack.
DMUL	Multiply NOS by TOS. Lower half of result to NOS. Pop Stack.
DMUU	Multiply NOS by TOS. Upper half of result to NOS. Pop Stack.
DDIV	Divide NOS by TOS. Result to NOS. Pop Stack.
FLOATING POINT 32 BIT	
FADD	Add TOS to NOS. Result to NOS. Pop Stack.
FSUB	Subtract TOS from NOS. Result to NOS. Pop Stack.
FMUL	Multiply NOS by TOS. Result to NOS. Pop Stack.
FDIV	Divide NOS by TOS. Result to NOS. Pop Stack.
DERIVED FLOATING POINT FUNCTIONS	
SQRT	Square Root of TOS. Result in TOS.
SIN	Sine of TOS. Result in TOS
COS	Cosine of TOS. Result in TOS.
TAN	Tangent of TOS. Result in TOS.
ASIN	Inverse Sine of TOS. Result in TOS.
ACOS	Inverse Cosine of TOS. Result in TOS.
ATAN	Inverse Tangent of TOS. Result in TOS.
DERIVED FLOATING POINT FUNCTIONS (Continued)	
LOG	Common Logarithm (base 10) of TOS. Result in TOS.
LN	Natural Logarithm (base e) of TOS. Result in TOS.
EXP	Exponential (e^x) of TOS. Result in TOS.
PWR	NOS raised to the power in TOS. Result in NOS. Pop Stack.
DATA MANIPULATION COMMANDS	
NOP	No Operation
FIXS	Convert TOS from floating point to 16-bit fixed point format.
FIXD	Convert TOS from floating point to 32-bit fixed point format.
FLTS	Convert TOS from 16-bit fixed point to floating point format.
FLTD	Convert TOS from 32-bit fixed point to floating point format.
CHSS	Change sign of 16-bit fixed point operand on TOS.
CHSD	Change sign of 32-bit fixed point operand on TOS.
CHSF	Change sign of floating point operand on TOS.
PTOS	Push 16-bit fixed point operand on TOS to NOS (Copy)
PTOD	Push 32-bit fixed point operand on TOS to NOS. (Copy)
PTOF	Push floating point operand on TOS to NOS. (Copy)
POPS	Pop 16-bit fixed point operand from TOS. NOS becomes TOS.
POPD	Pop 32-bit fixed point operand from TOS. NOS becomes TOS.
POPF	Pop floating point operand from TOS. NOS becomes TOS.
XCHS	Exchange 16-bit fixed point operands TOS and NOS.
XCHD	Exchange 32-bit fixed point operands TOS and NOS.
XCHF	Exchange floating point operands TOS and NOS.
PUPI	Push floating point constant "π" onto TOS. Previous TOS becomes NOS.

NOTE: TOS means Top of Stack. NOS means Next on Stack.
POP means remove from stack and rotate stack.
PUSH means deposit on stack and rotate stack.

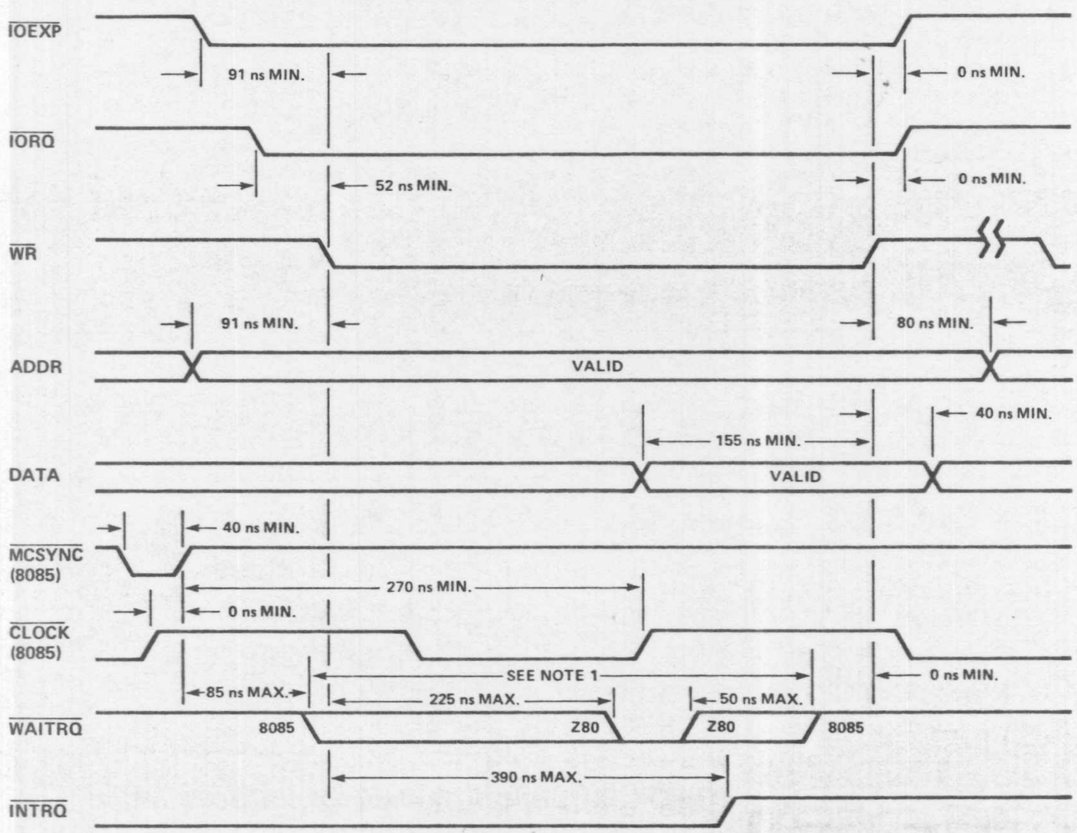
TABLE 5. ISB-3600 DC Characteristics

PARAMETER	LIMITS
Power V_{CC}	+5V ±5%
Power V_{DD}	+12V ±5%
BUS Input Loading	1 LS Load max.
BUS Output Drive	60 LS* Loads max.
BUS Tri-State Leakage	1 LS* Load max.

*Low-power Schottky

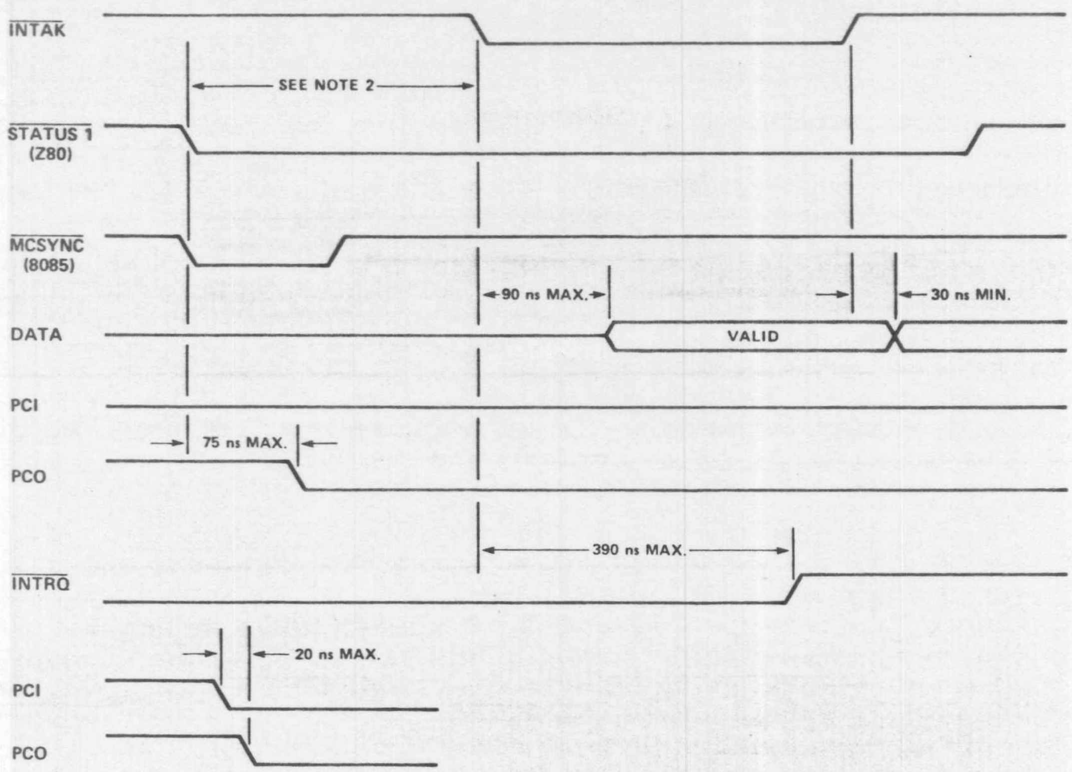


READ



WRITE

FIGURE 3. ISB-3600 Timing Diagrams



INTERRUPT

NOTE 1. During a read cycle, the ISB-3600 will generate wait states. The $\overline{\text{WAITRQ}}$ pulse width will be approximately the value shown below:

CYCLE	
Read DATA Z80	3.05 μs max.
Read Status Z80	1.76 μs max.
Write 8085	370ns max. with a 3 MHz clock for CPU
Read Data 8085	3.05 μs max.
Read Status 8085	1.76 μs max

NOTE 2. The negative edge of $\overline{\text{MCSYNC}}$ (8085) and $\overline{\text{STATUS 1}}$ (Z80) is used to determine priority when vectored interrupts are used. The earlier these lines go low, the longer the priority chain time out can be. Therefore, you can have more boards involved in the priority chain. For example, if every card delayed, the priority chain by 20ns max. (one gate delay) you could put 6 cards in the priority chain with $\overline{\text{STATUS 1}}$ or $\overline{\text{MCSYNC}}$ going low 100ns before $\overline{\text{INTAK}}$.

FIGURE 3. ISB-3600 Timing Diagram (Continued)

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